

Preliminary Amendment

Applicant: Werner Ertle et al.

Serial No.: Unknown

(Priority Application No. DE 102 34 648.8)

(International Application No. PCT/DE03/02544)

Filed: Herewith

(Priority Date 29 July 2002)

(International Filing Date 29 July 2003)

Docket No. I431.124.101/FIN 404 PCT/US

Title: SEMICONDUCTOR WAFER WITH ELECTRICALLY CONNECTED CONTACT AND TEST AREAS

IN THE ABSTRACT

Please replace the Abstract with the following rewritten paragraph:

Abstract

~~Arrangement of contact areas and test areas on patterned semiconductor chips~~
SEMICONDUCTOR WAFER WITH ELECTRICALLY CONNECTED CONTACT AND TEST AREAS

Abstract

The invention relates to an arrangement of contact areas-(1) and test areas-(2) on patterned semiconductor chips-(3). The contact areas-(1) and the test areas-(2) are electrically connected to one another via a conduction web-(4). Whereas the contact areas-(1) are arranged in a first region-(5), which has no components of an integrated circuit, the test areas (2) lie in a second region-(7) of the top side of the semiconductor chip-(3), which region has components-(6) of an integrated circuit.

{figure 1}